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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,060	01/02/2002	Sujat Jamil	42390P12483	9109

8791 7590 06/28/2005

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EXAMINER	
LANE, JOHN A	
ART UNIT	**PAPER NUMBER**
2188	

DATE MAILED: 06/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,060	JAMIL ET AL.	
	Examiner	Art Unit	
	Jack A. Lane	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office action is responsive to the amendment filed 06/02/2005. Claims 1-26 are presented for examination. Any objections or rejections made in the previous office action not specifically repeated below are withdrawn or have been overcome by applicant's response.

2. Applicant has not responded to the request for information on two prior occasions. The request is provided once again to give applicant the opportunity to respond. The examiner requests, in response to this Office action, any documentation known to qualify as prior art under 35 U.S.C. sections 102 or 103 with respect to the invention as defined by the independent and dependent claims. That is, any prior art (including any documentation used to develop the disclosed/claimed subject matter, background art and any products for sale) similar to the claimed invention that could reasonably be used in a 102 or 103 rejection. This request does not require applicant to perform a search. Support for this request is derived from 37 C.F.R. 1.56 and 1.105, however, it is not intended to interfere with or go beyond that **required** under 37 C.F.R. 1.56 or 1.105.

The request may be fulfilled by asking the attorney(s) of record handling prosecution and the inventor(s)/assignee for references qualifying as prior art. A simple statement that the query has been made and no prior art found is sufficient to fulfill the request. Otherwise, the fee and certification requirements of 37 CFR section 1.97 are waived for those documents submitted in reply to this request. This waiver extends only to those documents within the scope of this request that are included in the applicant's first complete communication responding to this

requirement. Any supplemental replies subsequent to the first communication responding to this request and any information disclosures beyond the scope of this request are subject to the fee and certification requirements of 37 CFR section 1.97.

In the event documentation (e.g. newly submitted/previously submitted on an IDS, incorporated by reference or "common knowledge" generally found in the background section but not a publication) is determined to qualify as prior art, a discussion of relevant passages, figs. etc. with respect to the claims must be provided. The examiner is looking for specific references to 102/103 prior art that identify independent and dependent claim limitations. Since applicant is most knowledgeable of the present invention and submitted art, a discussion of the reference(s) with respect to the instant claims is essential.

In the present application, an Exhibit A (filed 02/15/2005) constituting an invention disclosure form is part of a 131 declaration to show prior invention. In Exhibit A, the following statement appears:

> The closest prior art we are aware of is the IBM Power 4, which is a 2-core CMP with a shared L2 cache, with each core containing private L1 caches. To our knowledge, IBM's public disclosures have not disclosed whether or how the cores transfer cache lines between the private core caches

Since the printing of Exhibit A, has the inventor, assignee or the present attorney(s) of record become aware of data transfers between private cache cores in the IBM Power 4 (or other IBM product)? A response to this inquiry is requested.

The examiner also requests, in response to this Office action, a showing of support for language added to any original claims on amendment and any new claims. That is, indicate

support for newly added claim language by specifically pointing to page(s) and line no(s). in the specification and/or drawing figure(s).

When responding to the Office action, Applicant is advised to clearly point out the patentable novelty the claims present in view of the state of the art disclosed by the reference(s) cited or the objections made. A showing of how the amendments avoid such references or objections must also be present. See 37 C.F.R. 1.111(c).

3. Claims 23-26 are not limited to tangible embodiments. In view of Applicant's disclosure, specification page 15, line 24 - page 16, line 2, the medium is not limited to tangible embodiments, instead being defined as including both tangible embodiments (e.g., read only memory (ROM); random access memory; magnetic disk storage media; optical storage media; flash memory devices) and intangible embodiments (e.g., electrical, optical, acoustical or other form of propagated signals, carrier waves, infrared signals, digital signals, etc). As such, the claim is not limited to statutory subject matter and is therefore non-statutory.

To overcome this type of 101 rejection the specification needs to be amended to include only the physical computer media and not a transmission media or other intangible or non-functional media.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary

skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. section 103 (a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 C.F.R. 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli (6,587,926) in view of the standard practice of integrating circuits, as further evidenced by Sherburne (2002/0184546).

Arimilli discloses a power supply, a plurality of processor units, a plurality of cache units, one of the cache units provided for each one of the processor units, an embedded RAM unit for storing instructions and data for the processor units (e.g., Figure 1), a cache coherent bus coupled to the processor units and the embedded RAM unit, the bus configured to provide cache coherent snooping commands from the processor units themselves (col. 9, lines 39-45) to ensure cache coherency between the cache units for the processor units and the embedded RAM unit (e.g., col. 2, lines 1-5). Arimilli does not expressly mention a particular embodiment of an integrated circuit die, however the Examiner takes Official Notice that it is manifestly obvious to integrate multi-processing devices for the well-known and well-noted advantages of portability, power consumption, and so forth. This is further evidenced by Sherburne. Sherburne discloses the well-known practice of using highly integrated devices to obtain the advantages of decreased size and weight (e.g., paragraph (0002)).

It would be obvious to combine Arimilli with the well-known practice of integration because the practice is standard and the advantages for doing so are well established in areas such as those evidenced by Sherburne, which included multiprocessing systems with cache and embedded memory. Therefore it would be obvious to one of ordinary skill in the art to combine Arimilli with the standard practice of integration.

The examiner believes all dependent claim features not specifically discussed above are expressly or inherently taught by Arimilli or Sherburne. The remaining dependent claim features, while part of the invention, do not appear essential to the main invention found in the independent claims. Thus, a detailed discussion of the well known claim feature(s) is not warranted at this time. Support for this line of reasoning is derived from 37 C.F.R. 1.105. 37 C.F.R. 1.105 permitting "stipulations as to facts" or "whether a dependent claim element is known in the prior art based on the examiner having a reasonable basis for believing so."

In the Remarks filed 06/02/2005, Applicant argues the following:

> As discussed above, neither Arimilli nor Sherburne disclose or suggest transferring a cache line from a first dedicated processor cache and to transfer the first cache line to a second dedicated processor cache. Arimilli discloses an architecture having dedicated processor caches. However, there is no disclosure of control logic that transfers cache lines between the dedicated processor caches.

In response, Arimilli states the following at col. 5, lines 59-62 with respect to figure 2:

> A cache controller 214 and queues 210 are incorporated within each of L1 caches 104a and 104b to facilitate data access transactions **between** processors 102a and 102b and processor bus 106a.

At col. 7, lines 36-43 and lines 51-54; col. 8, lines 38-46 and col. 9, lines 33-45 the following is stated with respect to cache to cache data transfers:

> With reference now to FIG. 4, there is illustrated a diagram of a storage device that eliminates the need for reserved vertical queuing of data access requests and provides for enhanced **scarfing** capability...The elements depicted are equally applicable in L2 caches 108a-108b, **L1 caches 104a-104b**, and L3 caches 110a-110n.
>
> Snoop logic 412 detects operations initiated by a **horizontal** storage device (i.e., another L2 cache for L2 caches 108a-108n, ...)
>
> "**scarfing**" refers to the capture of retrieved data by a data storage device...(i.e. not a requestor or a necessary recipient of the target data). Such a device will be referred to herein as a "**third party transactor**"... Situations in which a data storage device acts as a **third party transactor** often arise in the context of **horizontal cache coherency.** Examples of cache coherency operations resulting in a storage device acting as a third party transactor which scarfs data are described in co-pending U.S. patent application No. 09/024,609 (now Patent No. 6,292,872).
>
> Referring to FIG. 6,...depicts a storage device snooping a data access response...the snooping device is a potential third party transactor, the scarf tag field designated for the memory level at which the snooper resides is compared with the snoopers device identification tag. If a match is found at step 610,...the snoop device writing the target data into its memory

As found in Arimilli (6,292,872) col. 6, lines 11-18 and 35-41:

> If however, the read request misses in both L1 cache 12a and L2 cache 14a, cache controller 36 of L2 cache 14a presents the read request as a transaction on interconnect 16, which is **snooped**...In response to **snooping** the read request..., cache controller 36...determines if the requested data is resident in...the associated one of L1 caches 12b-12n.
>
> If the data requested...is stored, for example, in L1 cache 12n..., cache controller 36...signals L1 cache 12n to push the requested data to L2 cache 14n . L2 cache 14n sources the requested data on interconnect 16 (*to the requesting processor*).

Given the above disclosure it is clear that snoop logic 412 and/or the cache controller of Arimilli corresponds to the claimed control logic and can transfer data (i.e. cache lines) between dedicated processor L1 caches (104a and 104b, 12a and 12b-n). That is, an L1 cache acting as a

third party transactor can snoop other L1 cache's to scarf data (i.e. transfer data from one cache to another) to maintain coherency (i.e. horizontal cache coherency).

6. Applicant's arguments filed 02/15/2005 with respect to claim 1-26 have been considered but are deemed to be moot in view of the new grounds of rejection.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 C.F.R. 1.136(a).

8. A SHORTENED STATUTORY PERIOD FOR RESPONSE TO THIS FINAL ACTION IS SET TO EXPIRE THREE MONTHS FROM THE DATE OF THIS ACTION. IN THE EVENT A FIRST RESPONSE IS FILED WITHIN TWO MONTHS OF THE MAILING DATE OF THIS FINAL ACTION AND THE ADVISORY ACTION IS NOT MAILED UNTIL AFTER THE END OF THE THREE-MONTH SHORTENED STATUTORY PERIOD, THEN THE SHORTENED STATUTORY PERIOD WILL EXPIRE ON THE DATE THE ADVISORY ACTION IS MAILED, AND ANY EXTENSION FEE PURSUANT TO 37 C.F.R. 1.136(a) WILL BE CALCULATED FROM THE MAILING DATE OF THE ADVISORY ACTION. IN NO EVENT WILL THE STATUTORY PERIOD FOR RESPONSE EXPIRE LATER THAN SIX MONTHS FROM THE DATE OF THIS FINAL ACTION.

Any response to this final action should be mailed to:
Box AF

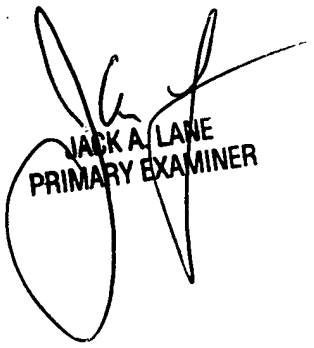
Under Secretary of Commerce for Intellectual Property and Director of the United States Patent and Trademark Office
PO Box 1450
Alexandria, VA 22313-1450
or faxed to:
(703) 872-9306, (for Official communications intended for entry)
Or:
(703) 872-9306, (for Non-Official or Draft communications, please label "Non-Official" or "DRAFT")

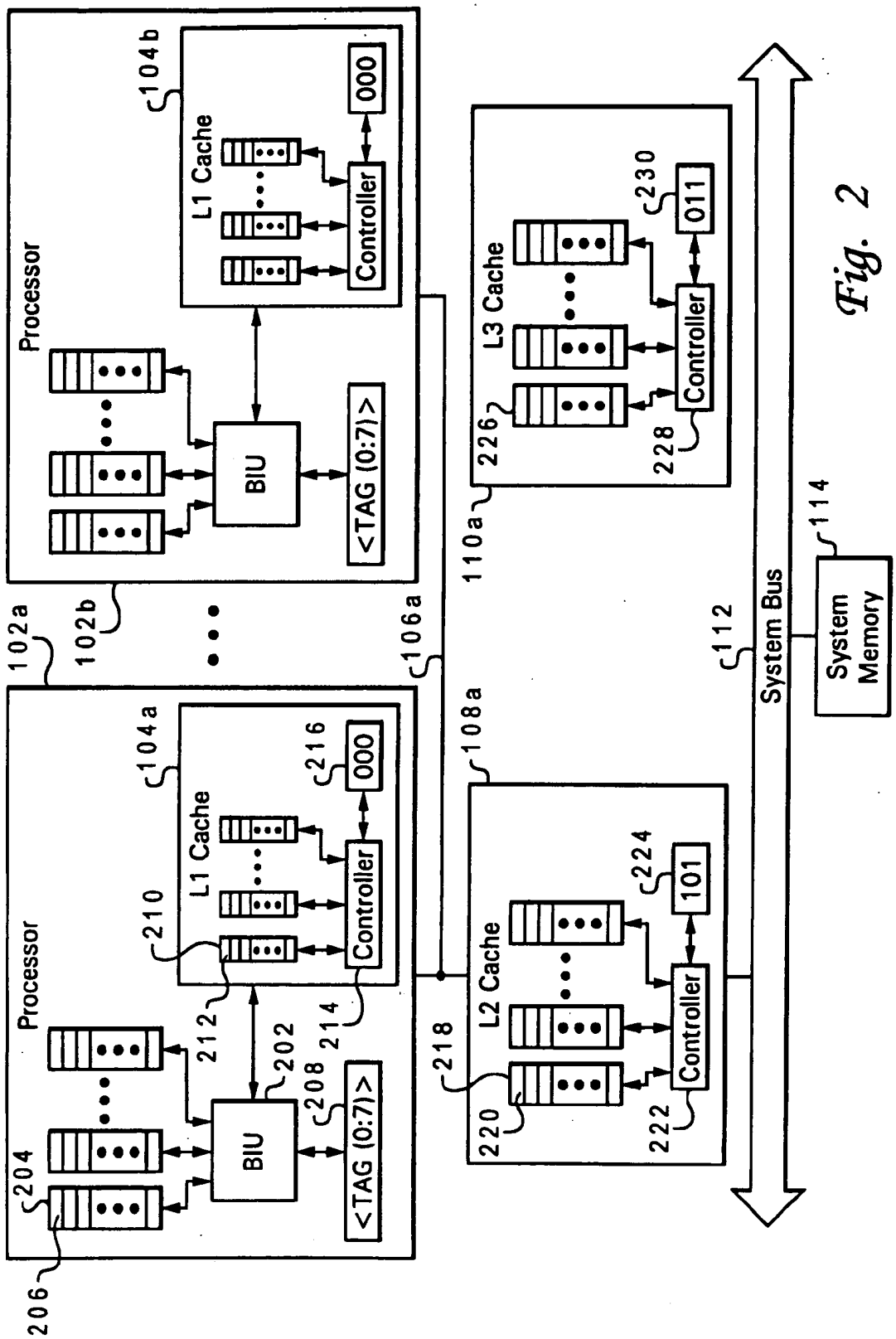
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack A. Lane whose telephone number is 571 272-4208. The examiner can normally be reached on Mon-Fri from 7:30AM-6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571 272-4210.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571 272-2100

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BIU
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101
L3 Cache
011
System Bus
System Memory
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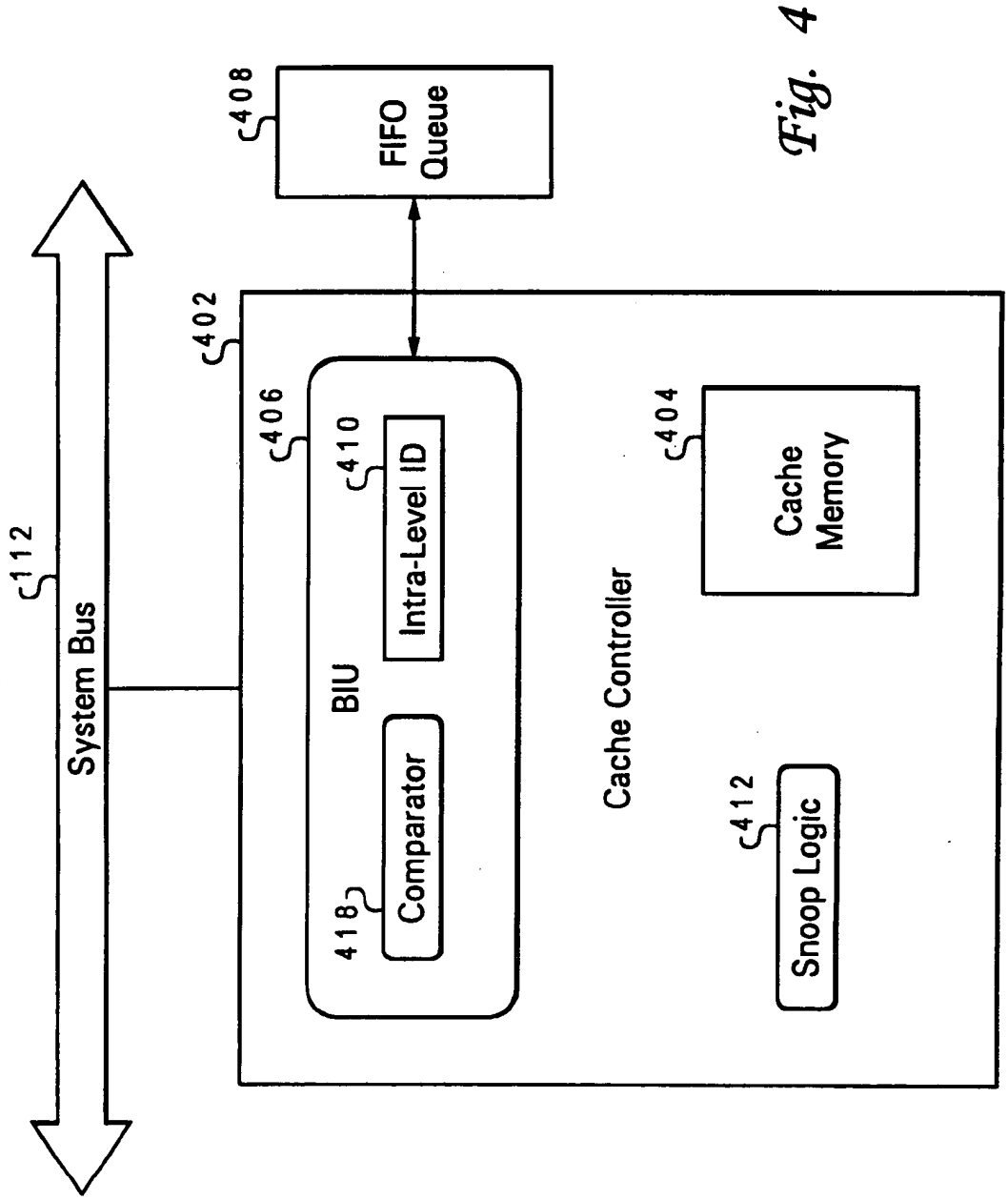
102b
104a
104b
106a
108a
110a
112
114
202
204
206
208
210
212
214
216
218
220
222
224
226
228
230

Fig. 2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402
406
410
Intra-Level ID
BIU
418
Comparator
404
Cache Memory
Cache Controller
412
Snoop Logic
112
System Bus

Fig. 4